PATENT APPLICATION

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE
BEFORE THE BOARD OF PATENT APPEALS AND INTERFERENCES

In re application of

Takao TOI

Appln. No.: 09/505,429

Confirmation No.: 7134

Filed: February 16, 2000

For: IMAGE PROCESSING SYSTEM

Docket No: Q57908

Group Art Unit: 2623

Examiner: Colin M. LAROSE

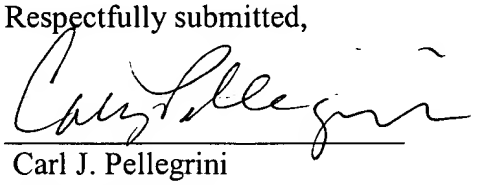
SUBMISSION OF APPEAL BRIEF

MAIL STOP APPEAL BRIEF - PATENTS
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

Submitted herewith please find an Appeal Brief. A check for the statutory fee of $340.00 is attached. The USPTO is directed and authorized to charge all required fees, except for the Issue Fee and the Publication Fee, to Deposit Account No. 19-4880. Please also credit any overpayments to said Deposit Account. A duplicate copy of this paper is attached.

Respectfully submitted,



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Date: November 12, 2004

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APPEAL BRIEF UNDER 37 C.F.R. § 41.37

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Sir:

In accordance with the provisions of 37 C.F.R. § 41.37, Appellant submits the following:

I. REAL PARTY IN INTEREST

The real party in interest in this appeal is NEC CORPORATION. Assignment of the application was submitted to the U.S. Patent and Trademark Office on February 16, 2000, and recorded on the same date at Reel 010600, Frame 0766.

II. RELATED APPEALS AND INTERFERENCES

There are no known appeals or interferences that will affect, be directly affected by, or have a bearing on the Board's decision in the pending appeal.

III. STATUS OF CLAIMS

Claims 1-22 stand finally rejected.

The rejections of claims 1-22 are being appeal.

IV. STATUS OF AMENDMENTS

No amendments have been filed subsequent to the final rejection.

V. SUMMARY OF THE CLAIMED SUBJECT MATTER

Appellant's claimed invention relates to an image processing system that processes image data from, for example, a digital still and/or video camera. Specification 1:2-6. More particularly, the image processing system has a field programmable gate array (FPGA) that is capable of altering an internal logic description prescribing a particular operation during an operating state. Specification, 3:23-26.

In the claimed invention, the FPGA is an array that is capable of configuring a dynamic reconfigurable system. The dynamic reconfigurable system enables wired logic to be altered arbitrarily and dynamically. The internal logic description is an application program that is written in the FPGA, or which is executed on the chip of the FPGA. Specification, 3:14-21.

Fig. 1 is a block diagram showing an exemplary embodiment of the claimed image processing system. The image processing system comprises a lens 100, a control circuit 101, a solid state image pick-up element 102, a drive circuit 103, an amplifier 104, an AD conversion circuit 105, an FPGA 106, a display device 107, a storage device 108 such as an EEPROM

(Electrically Erasable Programmable Read-Only Memory), a RAM (Random Access Memory) 109, and an external equipment 110. Specification, 6:19-27.

During operation, light permeates lens 100 and undergoes photoelectric conversion at solid state image pick-up element 102. Lens 100 is controlled by the control circuit 101. Solid state image pick-up element 102 is driven by the drive circuit 103. Amplifier 104 controls the gain of an analog image output signal of solid state image pick-up element 102. The AD conversion circuit converts the image output signal of amplifier 104 into a digital signal by AD conversion circuit 105. FPGA 106 receives the digital image signal of AD conversion circuit 105 and executes image processing. The operation of FPGA 106 is determined by the internal logic description (or application program). Storage device 108 stores the internal logic description of FPGA 106. External equipment 110 is capable of rewriting the data of storage device 108 or the internal logic description of FPGA 106. Specification, 6:28-7:16.

Next, an example of a digital camera with an image compression function will be described. The internal logic description of FPGA 106 is transferred during operation from storage device 108 or a storage device provided on the inside of FPGA 106. The image processing system picks up an image during image pick-up mode. The image processing system executes color separation processing during the interval of an active pixel. In an interval of a non-active pixel, with the exception of the interval of an active pixel, the image processing system rewrites the internal logic description of FPGA 106 to an internal logic description for controlling the camera. Then, the image processing system executes automatic control, such as an

automatic white balance control processing, an auto-focus control processing, or an automatic lightness control processing. Specification 7:17-29.

Subsequently, the image processing system rewrites the internal logic description of the FPGA 106 to the internal logic description for performing the color separation processing again. As shown in Fig. 2, the horizontal blanking interval, vertical blanking interval, optical black pixel interval and so forth, mean the scanning interval of an active pixel of the image pick-up element. Consequently, the interval of a non-active pixel, with the exception of the interval of an active pixel, means the scanning interval, with the exception of the interval of an active pixel of the image pick-up elements, such as the horizontal blanking interval, the vertical blanking interval, the optical black pixel interval, and so forth. When the camera shutter is pressed, or an image is recorded, the internal logic description of FPGA 106 is rewritten to the internal logic description for performing image compression processing. External equipment 110 is connected to the image processing system. The image processing system receives an instruction that the image is transferred. The image processing system enters a transferring mode. Furthermore, external equipment 110 is connected to the image processing system before an instruction that the internal logic description is updated is given. The image processing system enters an updating mode. Fig. 3 shows the state of the respective modes. Specification, 7:30-8:19.

VI. GROUNDS OF REJECTION TO BE REVIEWED ON APPEAL

Appellant appeals the rejection of claims 1-4, 7-10, 11-14 and 17-22 under 35 U.S.C. § 103(a) as being unpatentable over Baxter et al. (U.S. Patent No. 5,486,853) and Kolchinsky (U.S. Patent No. 5,301,344).

Appellant also appeals the rejection of claims 5, 6, 15 and 16, which have been rejected under 35 U.S.C. § 103(a) as being unpatentable over Baxter et al. and Kolchinsky, and further in view of Fukuoka (5,754,227).

VII. ARGUMENTS

A. The Rejections of Claims 1-20

Appellant respectfully requests the members of the Board to reverse the aforementioned rejections of claim 1-20 under 35 U.S.C. § 103(a) because the cited references fail to disclose or suggest all of the claim limitations. Specifically, the references fail to disclose or suggest at least the following limitations of independent claims 1 and 11:

> executing digital image processing of an interval of active pixel in the condition that a first internal logic description is written in said field programmable gate array;
>
> executing digital control processing in the condition that said first internal logic description of said field programmable gate array is rewritten to a second internal logic description in an interval of non-active pixel with the exception of said interval of active pixel; and
>
> executing digital image processing again in the condition that said second internal description is rewritten to said first internal logic description;

Appellant first notes that the Examiner concedes that Baxter et al. fails to disclose an FPGA for executing the image and control processing wherein the first and second internal logic descriptions, corresponding to each type of processing, are written to the FPGA. 5/12/04 Office Action (paper no. 15), page 3. Instead, the Examiner asserts that Baxter et al. discloses using dedicated processors 66 and 70 for executing each type of processing.

In order to make up for this deficiency, the Examiner cites to Kolchinsky. Specifically, the Examiner asserts that Kolchinsky discloses a reconfigurable image processing system (figure 2) that is implemented by case address generator 22 and arithmetic unit 26 (see figure 2), wherein arithmetic unit 26 operates to process image data. The Examiner also asserts that Kolchinsky discloses that both image processing (e.g., image compression, color processing) and control processing (e.g., zooming/panning) are executed by the arithmetic unit 26 (figure 2). 5/12/04 Office Action (paper no. 15), page 4.

However, Kolchinsky does not disclose or suggest using an FPGA to perform digital control processing. Therefore, one of skill in the art would not have been motivated to replace Baxter et al. processor 70 (which performs control processing) with an FPGA. The reference to "zooming/panning" in Kolchinsky figure 4 is not an example of the claimed digital control processing. The claimed digital control processing relates to control of the image system, rather than to processing of the image captured by the system. Examples of digital control processing include adjusting white balance, auto-focusing and controlling light. Specification, 7:27-29. On the other hand, the "zooming/panning" in Kolchinsky relates to manipulation of the captured image, not to control of the system.

Appellant also notes that in Baxter et al., the camera is controlled during a non-active pixel period. Two separate devices, CPU lens control exposure control 70 and digital camera processor 66, serve as the controller for the camera. Baxter et al. does not disclose that CPU 70 is used for other image processing during an active pixel period. Nor does Baxter et al. disclose that processor 66 is used to control the camera. Figures 8 and 9 do not show any arrowhead from the processor 66 to the camera head.

The claimed invention, on the other hand, uses an FPGA for both image processing and controlling the camera. Image processing is performed during an active pixel period and control processing is performed during a non-active pixel period.

Also, the camera head in Baxter et al. is separated from the main body. This is because the digital camera processor 66 must execute processes faster, and CPU 70, which is a general purpose processor, is not suitable for controlling the camera. Therefore, in order to combine processor 66 and CPU 70, it would be necessary to use a wired logic processing device, such as an ASIC, instead of a general purpose CPU.

Regarding claims 2-10 and 12-20, they should be allowable at least based on their dependence from claims 1 or 11 for at least the same reasons.

B. The Rejection of Claim 21

Appellant respectfully requests the members of the Board to reverse the aforementioned rejection of claim 21 under 35 U.S.C. § 103(a) because the cited references fails to disclose or suggest all of the claim limitations.

First, claim 21 contains the following limitations which are similar to the limitations in claims 1 and 11 discussed above in section A:

> executing digital image processing of an interval of active pixel in the condition that a first internal logic description is written in said field programmable gate array;
>
> executing digital control pre-processing or post-processing relating to said image processing in the condition that said first internal logic description of said field programmable gate array is rewritten to a second internal logic description in an interval of non-active pixel with the exception of said interval of active pixel; and
>
> executing digital image processing again in the condition that said second internal description is rewritten to said first internal logic description.

Therefore, claim 21 should be allowable for the same reasons as claims 1 and 11. In addition, claim 21 requires that the control processing is pre-processing or post-processing relating to said image processing. This limitation is not disclosed or suggested in any of the cited references.

C. The Rejection of Claim 22

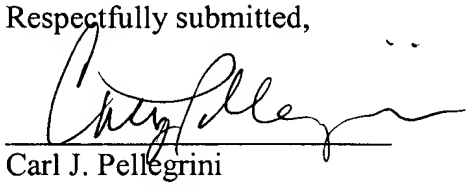
Appellants respectfully request the members of the Board to reverse the aforementioned rejection of claim 22 under 35 U.S.C. § 103(a) because the cited references fails to disclose or suggest all of the claim limitations.

Claim 22 depends from claim 21. Therefore, it should be allowable at least for the same reasons as claim 21 described in section B. In addition, claim 22 also requires that the control and image processing occur in the same frame. This limitation is not disclosed or suggested in the cited references.

Unless a check is submitted herewith for the fee required under 37 C.F.R. §41.37(a) and 1.17(c), please charge said fee to Deposit Account No. 19-4880.

The USPTO is directed and authorized to charge all required fees, except for the Issue Fee and the Publication Fee, to Deposit Account No. 19-4880. Please also credit any overpayments to said Deposit Account.

Respectfully submitted,



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Date: November 12, 2004

CLAIMS APPENDIX

CLAIMS 1-22 ON APPEAL:

1. An image processing system provided with a field programmable gate array which is capable of altering an internal logic description, said description prescribing operation during an operating state, wherein an image processing method of said image processing system comprises:

executing digital image processing of an interval of active pixel in the condition that a first internal logic description is written in said field programmable gate array;

executing digital control processing in the condition that said first internal logic description of said field programmable gate array is rewritten to a second internal logic description in an interval of non-active pixel with the exception of said interval of active pixel; and

executing digital image processing again in the condition that said second internal description is rewritten to said first internal logic description;

wherein all operations necessary to perform said digital image processing and said digital control processing are performed in said field programmable gate array.

2. An image processing system as claimed in claim 1, wherein there is provided an image pick-up element, and said image processing system executes color signal processing of picked-up image by said image pick-up element during said interval of active pixel, while

during said interval of non-active pixel, said image processing system executes said digital control processing in relation to said color signal processing.

3. An image processing system as claimed in claim 1, wherein said interval of non-active pixel is a vertical blanking interval.

4. An image processing system as claimed in claim 1, wherein said interval of non-active pixel is a horizontal blanking interval.

5. An image processing system as claimed in claim 1, wherein said image processing system executes image compression processing in said interval of active pixel, and said image processing system executes digital control processing in relation to said image compression processing in said interval of non-active pixel.

6. An image processing system as claimed in claim 1, wherein said digital control processing is code quantity control processing.

7. An image processing system as claimed in claim 2, wherein said interval of non-active pixel is a interval of optical black pixel of said image pick-up element.

8. An image processing system as claimed in claim 2, wherein said digital control processing is an automatic white balance control processing.

9. An image processing system as claimed in claim 2, wherein said digital control processing is an auto-focus control processing.

10. An image processing system as claimed in claim 2, wherein said digital control processing is an automatic lightness control processing.

11. An image processing method for altering an internal logic description prescribing operation during an operating state comprising:

executing digital image processing of an interval of active pixel in the condition that a first internal logic description is written in a field programmable gate array;

executing digital control processing in the condition that said first internal logic description of said field programmable gate array is rewritten to a second internal logic description in an interval of non-active pixel with the exception of said interval of active pixel; and

executing digital image processing again in the condition that said second internal description is rewritten to said first internal logic description;

wherein all operations necessary to perform said digital image processing and said digital control processing are performed in said field programmable gate array.

12. An image processing method as claimed in claim 11, further comprising:

executing color signal processing of an image picked up by an image pick-up element during said interval of active pixel; and

executing said digital control processing in relation to said color signal processing during said interval of non-active pixel.

13. An image processing method as claimed in claim 11, wherein said interval of non-active pixel is a vertical blanking interval.

14. An image processing method as claimed in claim 11, wherein said interval of non-active pixel is a horizontal blanking interval.

15. An image processing method as claimed in claim 11, further comprising:

executing image compression processing in said interval of active pixel; and

executing digital control processing in relation to said image compression processing in said interval of non-active pixel.

16. An image processing method as claimed in claim 11, wherein said digital control processing is code quantity control processing.

17. An image processing method as claimed in claim 12, wherein said interval of non-active pixel is an interval of optical black pixel of said image pick-up element.

18. An image processing method as claimed in claim 12, wherein said digital control processing is an automatic white balance control processing.

19. An image processing method as claimed in claim 12, wherein said digital control processing is an auto-focus control processing.

20. An image processing method as claimed in claim 12, wherein said digital control processing is an automatic lightness control processing.

21. An image processing system provided with a field programmable gate array which is capable of altering an internal logic description, said description prescribing operation during an operating state, wherein an image processing method of said image processing system comprises:

executing digital image processing of an interval of active pixel in the condition that a first internal logic description is written in said field programmable gate array;

executing digital control pre-processing or post-processing relating to said image processing in the condition that said first internal logic description of said field programmable gate array is rewritten to a second internal logic description in an interval of non-active pixel with the exception of said interval of active pixel; and

executing digital image processing again in the condition that said second internal description is rewritten to said first internal logic description.

22. An image processing system as claimed in claim 21, wherein said digital image processing and said digital control pre-processing or post-processing occur in one frame.

EVIDENCE APPENDIX:

None.

RELATED PROCEEDINGS APPENDIX

None.